# MIXED-CRITICALITY REAL-TIME SYSTEMS

**21st to 25th May, 2018**

## Overview

Methodologies that are currently used widely in the design and implementation of safety-critical real-time application systems are primarily focused on ensuring correctness. This, in conjunction with the trend towards implementing such systems using COTS components, may lead to very poor utilization of the implementation platform resources during runtime. Mixed-criticality implementations have been proposed as a means of achieving more efficient resource utilization upon such platforms, whereby highly safety critical functionalities are implemented upon the same platform as less critical functionalities. Informally speaking, the idea is that the resources which are provisioned to highly critical functionalities during design time, but are likely to remain unused by these functionalities at run-time, can be "re-claimed" and used to make performance guarantees, albeit at lower levels of assurance, to the less critical functionalities. The real-time scheduling community has been developing a theory of mixed-criticality scheduling that seeks to solve resource allocation problems for mixed-criticality systems, thereby significantly enhancing our ability to design and implement large, complex, real-time systems in a manner that is both provably correct and resource-efficient. The course will include case studies concerning design issues in modern mixed-criticality systems like Unmanned Aerial Vehicles (UAVs), Automotive Systems, Railway Systems etc.

**Objectives**

The primary objectives of the course are as follows:

1. To introduce the fundamentals of real-time scheduling theory, with a strong emphasis on the application of this theory to the design and analysis of mixed-criticality systems.

2. To provide an overview of the current state of the art of mixed-criticality scheduling theory, as well as advanced research initiatives. Case studies related to design issues in modern mixed-criticality systems like UAVs and automotive systems will be discussed and handled.

3. To provide exposure to important open problems and research questions in mixed-criticality systems design, implementation and analysis.

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| **Tentative Schedule** | **21st to 25th May, 2018**<br><br>**Day 1**: Introduction to real-time scheduling **(2 hrs lecture (AS), 2 hrs tutorial (SB))**<br><br>**Day 2**: Introduction to mixed-criticality scheduling. Mixed-criticality scheduling of independent jobs on uniprocessor platforms: Worst-Case Reservation Scheduling, Own-Criticality-Based-Priority Algorithm, Schedulability Test, Speed-Ups **(2 hrs lecture (SKB), 1 hr lecture (AS), 1 hr tutorial (SKB))**<br><br>**Day 3**: Mixed-criticality scheduling of recurrent tasks on uniprocessors: Scheduling for implicit-deadline and arbitrary-deadline tasks, Schedulability test, Speed-Ups **(2 hrs lecture (SKB), 1 hr lecture (SB), 1 hr tutorial (SKB))**<br><br>**Day 4**: Mixed-criticality scheduling on multiprocessors: Global and partitioned scheduling approaches **(2 hrs lecture (SKB), 2 hrs tutorial (SKB))**<br><br>**Day 5**: Recent research and Open problems: Review **(2 hrs lecture (SKB), 1 hr lecture (AS), 1 hr lecture (SB))**<br><br>Prof. Sanjoy Baruah (SKB): 08 hrs lectures and 04 hrs tutorials<br>Dr. Arnab Sarkar (AS): 04 hrs lectures<br>Dr. Santosh Biswas(SB): 02 hrs lectures and 02 hrs tutorials |
| **You Should Attend If…** | ▪ Executives, engineers and researchers from manufacturing, service and government organizations including R&D laboratories.<br><br>▪ Student students at all levels (BTech/MSc/MTech/PhD) or Faculty from reputed academic institutions and technical institutions. |
| **Fees** | The participation fees for taking the course is as follows:<br>**Industry/ Research Organizations: 15,000.00 INR**<br>**Faculty from Academic Institutions: 4000 INR**<br>**Students: 1000 (as caution money, refundable on successful completion of the course)**<br>The above fee include all instructional materials, computer use for tutorials and assignments, laboratory equipment usage charges, 24 hr free internet facility. The participants will be provided with accommodation on payment basis. |

# The Faculty

Prof. Baruah has completed PhD and MS from The University of Texas at Austin in 199 and 1989, respectively. He has obtained his B. Tech from The Indian Institute of Technology – Delhi in 1987. Professor Baruah has joined the Washington University in St. Louis in September 2017. He was previously at the University of North Carolina at Chapel Hill (1999-2017) and the University of Vermont (1993-1999). His research interests and activities are in real-time and safety-critical system design, scheduling theory, resource allocation and sharing in distributed computing environments, and algorithm design and analysis. He is a Fellow of the IEEE, and the recipient of the 2014 Outstanding Technical Contributions and Leadership Award of the IEEE Technical Committee on Real-Time Systems.

Arnaarkar received B.Tech in Information Technology (2003) from Calcutta University, Kolkata and his M.S (2006) and Ph.D (2012) degrees from the Department of Computer Science and Engineering at IIT Kharagpur. After submitting PhD in 2011, he worked briefly as a Visiting Scientist with the Advanced Computing and Micro-electronics Unit (ACMU), Indian Statistical Institute (ISI), Kolkata, India, before joining Samsung India Software Operations (SISO), Bangalore, where he worked for one year as a Chief Engineer with the Android Platforms Group. He is currently working as an Assistant Professor with the Department of Computer Science and Engineering, Indian Institute of Technology (IIT) Guwahati, India. His current research interests Real-time Scheduling, Bandwidth Allocation in Wireless Cellular Networks and Algorithms for Smart Grids.

Santosh Biswas received the B.E. degree from the National Institute of Technology Durgapur in the year 2001. He has completed his MS from the Department of Electrical Engineering, Indian Institute of Technology Kharagpur with highest institute CGPA in the year 2004. He obtained his PhD from the Department of Computer Science and Engineering, Indian Institute of Technology Kharagpur in the year 2008. He joined the Department of Computer Science and Engineering, Indian Institute of Technology Guwahati in 2009 and is currently an Associate Professor. His research interests include VLSI Testing and Design for Testability, Fault Tolerance, Network Security, Discrete-event systems and embedded systems. He has published about 130 research papers. He is a member of IEEE.

# Course Co-ordinators

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