

Ultra-Large-Scale Integration (ULSI) Technology and Nanoelectronic Devices

Overview

The advances in ultra-large-scale-integration (ULSI) technology based on aggressive scaling of CMOS devices provide enormous opportunities for high-performance communication, and computing systems. However, new device structures and designs are essential, as the scaling of devices is approaching its limit. This course is designed to provide the current status of advanced ULSI technology and projecting a roadmap for nanoelectronic devices for the next generation. The recent advances in nanotechnology for the growth and fabrication of nanometer-scale structures provide opportunities for novel electronic and photonic devices. The course lectures will cover several illustrative device examples drawn from semiconductor heterojunctions, strained layer epitaxy, and nanotechnology using both bottom-up and top-down approaches. Technology and applications of novel devices such as resonant tunneling diodes, single electron transistors, nanowire FETs and quantum dot memory will be discussed. A brief review of the emerging nano-devices using 2D semiconductors and spintronic materials will also be made. Lectures will be delivered by international renowned faculties from USA and India. Upon completion of the course, participants will acquire a broad knowledge of the state-of-the-art technology and applications of semiconductor nanodevices.

Course participants will learn the topics through lectures and laboratory visits. Assignments will be shared to stimulate research motivation of participants.

Modules	A: ULSI Technology & Nanostructures : Dec. 19 – Dec. 21 B: Nanoelectronic Devices : Dec. 22 – Dec. 24 Number of participants for the course will be limited to fifty.
Who Should Attend	<ul style="list-style-type: none"> ▪ The course is designed for B.Tech. / M.Sc. / M.Tech. and PhD students of Electronics, Electrical, Computer Science, Nanotechnology, Physics and Materials Science interested in the area of VLSI technology, semiconductor devices and nanotechnology. ▪ Scientists, Faculty members and Engineers from reputed academic institutions, R & D labs. and industrial participants working on semiconductor and photonic devices
Fees	The participation fees for taking the course is as follows: Participants from abroad : US \$500 Industry/ Research Organizations: 20000 Academic Institutions: 10000 Bonafide students of Academic Institutions: 1000 (to be refunded after completion of course) The above fee include all instructional materials, computer use for tutorials and assignments, laboratory equipment usage charges, 24 hr free internet facility. The participants will be provided with accommodation on payment basis.

The Faculty



Prof. Sanjay Banerjee is the Cockrell Family Regents Chair Professor and the Director of the Microelectronics Research Center in the Department of Electrical & Computer Engineering at The University of Texas at Austin, USA. Prof. Banerjee has over 530 archival refereed publications/talks, 7 books/chapters, and 26 U.S. patents. He is a Fellow of IEEE, Distinguished Lecturer for IEEE Electron Devices Society, and is the recipient of prestigious IEEE Andrew S. Grove Award 2014 for his "Outstanding contributions to Solid-state Devices and Technology". He is currently active in the areas of MOS and nanostructure Device Modeling, UHVCVD for silicon-germanium-carbon heterostructures and ultra-shallow junction technology and process modeling.



Prof. Samit K. Ray is the Head, School of Nanoscience and Technology and Professor, Department of Physics, IIT Kharagpur. His research interests are in the area of semiconductor nanostructures, quantum Dots, nanodevices and electronic materials. He has served as a visiting Professor / Scientist at the Tokyo Institute of Technology, Japan, University of Delaware, Newark, USA, University of Texas, Austin, USA, Max-Planck Institute for Solid State Research, Germany, Queen's University of Belfast, UK and National Taiwan University, Taiwan. Prof Ray has published more than 185 research papers in peer reviewed journals, six book chapters and co-authored a book on "Strained Silicon Heterostructures: Materials and Devices" published by IEE, UK.

Course Co-ordinator

Prof. Samit K Ray

Phone: 03222-283838

E-mail: physkr@phy.iitkgp.ernet.in

<http://www.gjan.iitkgp.ac.in/>