# Asynchronous and Synchronous approaches to Network-on-chip (NoC) Architecture design

## June 7-18, 2016

# Overview

This course will cover two new topics in the area of VLSI design – Asynchronous circuit design and design of Network-on-chip (NoC) architectures. Conventionally, processor architecture design is carried out using the synchronous design approach. However, technology scaling has paved the way for complex, high performance, multi-core processor architectures which cannot be designed using conventional synchronous approaches. In this course, we will compare and contrast different aspects of synchronous and asynchronous designs, provide an overview of both design styles, cover the design techniques used in asynchronous designs in detail and discuss in detail several aspects of NoC architectures, including router and network interface design, routing algorithms, and performance analysis of NoC architectures.

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| **Modules** | • **Synchronous and asynchronous design styles: Design of synchronous sequential datapath designs, asynchronous channels and pipelines, bundled data and QDI designs, multi-synchronous design and globally-asynchronous locally-synchronous (GALS) designs, metastability and synchronizers**<br>• **Network-on-Chip (NoC) architectures: NoC router designs, network interface design, routing algorithms, NoC simulators, asynchronous NoCs, case study examples.**<br>• **Labs will include hands-on sessions on FPGA programming, SystemVerilogCSP, demo session on NoC simulators and NoC design in FPGA and in Cadence Encounter.**<br>**Number of participants for the course will be limited to fifty.**<br>**More details on the course can be found at : http://www.iitgn.ac.in/gian/courses_noc.php** |
| **You Should Attend If…** | ▪ You are an engineer and researcher in the area of VLSI (Digital) design<br>▪ You are a post-graduate student or BTech student with exposure to VLSI Design or equivalent course.<br>▪ You are a faculty of reputed academic institute or researcher in government organizations including R&D laboratories. |
| **Fees** | The participation fees for taking the course is as follows:<br>• **Participants from abroad : US $200**<br>• **Industry/ Research Organizations: Rs. 5000/-**<br>• **Faculty : Rs. 2000/-**<br>• **Students : Rs. 500/-**<br>The above fee includes all instructional materials, computer use for tutorials, 24 hr free internet facility. The participants will be provided with accommodation on payment basis. |

# The Faculty

### Peter A. Beerel, Ph.D.

Prof. Peter Beerel is an Associate Professor in Electrical Engineering at University of South California, USA. Prof. Beerel received his B.S.E. degree in Electrical Engineering from Princeton University, Princeton, NJ, in 1989 and his M.S. and Ph.D. degrees in Electrical Engineering from Stanford University, Stanford, CA, in 1991 and 1994, respectively. He joined the the Department of Electrical Engineering--Systems at USC in 1994. Prof. Beerel is currently also the Faculty Director of Innovation and Entrepreneurship in Engineering for the Viterbi School of Engineering.

Prof. Beerel's research interests include a variety of topics in CAD and asynchronous VLSI design. He co-founded TimeLess Design Automation in 2008 which was acquired in 2010. He worked as Chief Scientist, Technology Development in the Communcation, Storage, and Infrastructure Group of Intel from 2011 to 2015. Prof. Beerel was a recipient of an Outstanding Teaching Award in 1997 and the Junior Research Award in 1998 and the Dean's Faculty Award for Service in 2011, all from USC's School of Engineering. He recieved a National Science Foundation (NSF) Career Award and a 1995 Zumberge Fellowship. He was the 2008 recipient of the IEEE Region 6 Outstanding Engineer Award for significantly advancing the application of asynchronous circuits to modern VLSI chips.

### Prof. Virendra Singh

Prof. Virendra Singh is a Faculty member at Indian Institute of Technology Bombay since Dec 2011. He received his Ph.D in Computer Science in 2005 from Nara Institute of Science and Technology (NAIST) Kansai. His research interests include Computer Architecture Processor architecture and micro-architecture, VLSI Testing, Fault-tolerant computing, Robustdesign and architectures, Self-healing system design, SoC/NoC design and test, Post Silicon Debug, High level synthesis, Formal verification. Before joining IITB, he was a faculty member at SERC, Indian Institute of Science (IISc), Bangalore from May 2007 - Dec 2011 and Scientist at Central Electronics Engineering Research Institute (CEERI), Pilani from Mar 1997 - May 2007.

### Dr. Joycee Mekie

Dr. Joycee Mekie received her PhD in Electrical Engineering from IIT Bombay in 2009. She has been faculty member at IIT Gandhinagar since Dec 2009. Her research interests include Asynchronous circuit design, Network-on-chip (NoC) architectures, Radiation hard designs and low-power VLSI design and Synchronizer studies.

## Course Co-ordinator

**Prof. Joycee Mekie**
**Assistant Professor,**
**Electrical Engineering**
**IIT Gandhinagar**
Phone: +91-89809 47993
E-mail: joycee@iitgn.ac.in

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http://www.iitgn.ac.in/faculty/electrical/joycee.htm