**Global Initiative of Academic Network (GIAN)**

(Faculty from outside India only can use this format)

Name of Faculty: Prof. Parthasarathi Roop

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New Zealand.

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Course Title: **The Science of Remulation for Executable Biology**

Broad Area: **Formal Methods in Computer Science with Bioengineering Focus**

**Overview:** Executable biology refers to executable computational models that mimic biological processes. Partha's group have recently proposed a refinement for real-time executable biology, where human organs can be transformed into executable models such that these models can operate in real-time with medical devices. The main motivation for such models is that they can be used for the validation of medical devices in a closed-loop without using live human organs. This has significant implications in medicine, biology, computer science, and also biomedical engineering. There are obvious implications for educational software related to this approach.

Closed-loop validation of controllers is well-known using emulation: hardware-in the loop simulation and model-in-the-loop validation. Here either the actual plant or its model may be used to validate the controller in closed-loop. Validation using the actual plant may not be practical in many situations such as live organs. Model-in-the-loop validation of human organs has received limited attention such computational models of organs provide high fidelity at the expense of very long simulation time. We propose the new approach of remulation to overcome these issues.

During emulation, the plant exists and the focus is the design of the controller. During remulation, we want to design a plant that can provide real-time response to a black-box controller. Hence, in this setting the plant controller relation ship is reversed and hence ***remulation is an acronym of reverse emulation***. A key requirement while developing remulation models is that the timing of the plant under design must be matched with that of the black-box controller. This design approach is extremely complex as the plant is typically a hybrid system, exhibiting both continuous dynamics and discrete mode switches.

We illustrate remulation by developing executable, real-time models of the cardiac conduction system of the human heart and illustrate the developed model in hardware as a remulated system for the validation of pacemakers.

**Objectives :**

The primary objectives of the course are as follows:

i) Comprehensive understanding of the models for biological systems such as the electrical conduction system of the human heart.

ii) Creating an awareness of the major challenges in the design of such systems, in particular the issues related to the cyber-physical nature of such systems.
iii) The use of formal methods and synchronous programming languages in the design of cyber-physical systems.
iv) Providing practical exposure to current design and research challenges of CPS, particularly related to executable biology.
v) Provide an inter-disciplinary focus where computer scientists, cardiac physicians, bioengineers and electrical engineers can cooperatively learn topics of immense interest for the design and verification of safety-critical systems used in medicine.

Tentative dates: **11 December-16 December**

**Course details:**

**Module A: Cyber-physical systems and Formal Methods**

**Lecture 1-2:**
This lecture will introduce key tenets of CPS and associated formal methods. It will introduce topics from closed-loop control systems, discrete event control, and real-time systems.

**Lecture 3-4: Background on embedded systems**
This lecture will provide an overview of the embedded system design flow and the current research questions of relevance to the topic of CPS. Topics covered will include techniques for synthesis, verification and static analysis of embedded systems.

**Lecture 5-6: The synchronous approach**
This lecture will focus on the well-known synchronous approach and its significance for the design of CPS. We will elaborate on tools such as Esterel, Scade (pure synchronous) and Zelus (hybrid). We will also present the approach used in Simulink / Stateflow from Mathworks.

**Lecture 7-8: Pacemaker and Timed Automata**

We will present well-known Pacemaker algorithms and illustrate formal modeling and validation of pacemakers using timed automata.

**Lecture 9-10: Models of the cardiac conduction system**

This will cover a range of models, form very high-fidelity bioengineering (finite element, finite volume) ones to more recent ones developed using timed and hybrid automata. We will illustrate the challenges of such modeling such as *scalability, timing and reentrancy*. Device specific behaviours such as the *restitution interval* and how to achieve good restitution will be discussed.

**Lab: Remulation-based validation of pacemakers**

Here Simulink and Piha will be introduced as tools for comparison and practical remulation examples will be demonstrated.

**References**


1. J. Fischer and T. Henzinger, Executable cell biology, *Nature Biotechnology* **25**, 1239 - 1249 (2007).
2. E. A. Lee, "Cyber Physical Systems: Design Challenges," in *Pro- ceedings of the 2008 11th IEEE Symposium on Object Oriented Real- Time Distributed Computing*, ISORC '08, (Washington, DC, USA), pp. 363–369, IEEE Computer Society, 2008.
3. R. Alur, *Principles of Cyber-Physical Systems*. MIT Press, 2015.
4. R. Wilhelm, J. Engblom, A. Ermedahl, N. Holsti, S. Thesing, D. Whalley, G. Bernat, C. Ferdinand, R. Heckmann, T. Mitra, F. Mueller, I. Puaut, P. Puschner, J. Staschulat, and P. Stenstro¨m, "The worst-case execution-time problem—overview of methods and survey of tools," *Trans. on Embedded Computing Systems, ACM*, vol. 7, no. 3, pp. 1–53, 2008.
5. International Electrotechnical Commission, "IEC 61508 Functional safety of electrical / electronic / programmable electronic safety- related systems." http://www.iec.ch/functionalsafety/.
6. R. Alur, C. Courcoubetis, T. A. Henzinger, and P.-H. Ho, "Hybrid Automata: An Algorithmic Approach to the Specification and Verification of Hybrid Systems," in *Hybrid Systems*, (London, UK), pp. 209–229, Springer-Verlag, 1993.
7. T. Bourke and M. Pouzet, "Zelus: a synchronous language with ODEs," in *Proceedings of the 16th international conference on Hybrid systems: computation and control*, pp. 113–118, ACM, 2013.
8. "Piha Tools from the University of Auckland." https://github.com/PRETgroup/PihaBenchmarks.
9. E. A. Lee et al. "Modeling and Simulating Cyber-Physical Systems using CyPhySim", ACM Embedded Software (EMSOFT) conference, 2015.
10. N Allen, S. Andalam, P. S. Roop, A. Malik, M. Trew and N. Patel, "Modular code generation for emulating the electrical conduction system of the human heart", Design Automation and Test in Europe (DATE), Dresden, Germany, 14-18 March 2016.
11. A. Malik, P. S. Roop, S. Andalam, E. Yip and M. Trew, "A synchronous rendering of hybrid systems for designing Plant-on-a-Chip (PoC)", arXiv preprint arXiv:1510.04336.


Here, 9-11 are key innovations that facilitate remulation.

**Teaching Faculty**

**Dr. Parthasarathi Roop and his Postdocs along with some cardiac physicians (to be named)**

**Bio:** Partha is an Associate Professor (equivalent to full-professor: www.eui.eu/ProgrammesAndFellowships/AcademicCareersObservatory/AcademicCare

ersbyCountry/Australia.aspx) in the Department of Electrical and Computer Engineering, University of Auckland, New Zealand.

He completed his PhD in Computer Science and Engineering at the University of New South Wales, Sydney, Australia, a M.Tech at Indian Institute of Technology in Kharagpur, India and a BE degree at Anna University (College of Engineering), Madras, India. Partha had visiting positions in Kiel University, Germany, French National Laboratory of Informatics and Control, and Iowa State University and University of California, Berkeley.

He has co-authored two research monographs and over one hundred papers, which includes a best paper award in embedded systems week (CASES 2013) and has recently received the Mercator professorship from the German Science Foundation (DFG), 2016. He has also received the Humboldt fellowship for experienced researchers in 2009. Partha is an Associate Editor of IEEE embedded systems letters and EURASIP Journal on Embedded Systems. He is in the TPC of leading conferences such as ACM EMSOFT and IEEE RTAS and is the PC co-chair of 19 IEEE ISORC to be held in York in May 2016.

**Who can attend:**

- Cardiac physicians particularly interested in cardiac devices such as pacemakers and other ICD devices. These can be members of private / public hospitals.
- This course is an ideal fit for members of the school of medical science and technology at IIT, Kharagpur and similar institutes.
- Computer science, electrical and bio-engineering professors and their graduate students.
- Students in computer science, bio-engineering and (MSc/MTech/PhD)

**Prerequisites**

The course has inter-disciplinary focus and will present material that is suitable for both computer scientists, engineers and cardiac and other physicians. For participants without computing / engineering background, we will offer help clinics.

**Tentative Schedule:** December 5-9, 2016

**Registration Fees**

| | | |
|---|---|---|
| Participants from abroad | : | US $100 |
| Industry/ Research Organizations: | : | Rs. 5000/- |
| Faculty members from Academic Institutions | : | Rs. 2500/- |
| Research Scholars/Postgraduate students | : | Rs 1000/- |
| Faculty/Research Scholars/Postgraduate students (MNIT) | : | NIL |
| Undergraduate students (in final year) (MNIT) | : | NIL |

The above fee includes all instructional materials, computer use for tutorials and free Internet facility. The participants will be provided with accommodation, if available, on payment basis.

**Proposed Budget**

| S.No | Description of budgetary head | Amount (Rs.) |
|---|---|---|
| 1 | (a) Air Fare (International Expert)<br>(b) Honorarium to Expert | 2,30,000 |
| 2 | Lecture Notes/video-learning material preparation | 1,50,000 |
| 3 | Contingency<br>(Boarding and lodging at MNIT guest house**, Visa fee, etc.) | 50,000 |
| 4 | Miscellaneous expenditure<br>(incl. Of Video recording expenses, if any)<br>(Item 1 to 4 should not exceed 8000 USD) | 50,000 |
| 5 | Host Faculty and/or Coordinator Honorarium* | |
| | GRAND TOTAL | 4,80,000 |

* Honorarium to course coordinator should be paid from the registrations received from the participants.

** In case of unavailability of the guest house, accommodation in an economy hotel as per provisions of 6CPC shall be arranged.

**Course Coordinators**


1. Dr. Lava Bhargava
   Associate Professor
   Department of Electronics and Communication Engineering
   Malaviya National Institute of Technology
   JLN Marg, Jaipur – 302017, India.
   Tel: +91 0141 2713337 (O)
   Email: lavab@mnit.ac.in

2. Dr. Vijay Laxmi
   Associate Professor
   Department of Computer Science and Engineering
   Malaviya National Institute of Technology Jaipur
   JLN Marg, Jaipur – 302017, India.
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# Partha S. Roop

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**Educational Qualifications:**

- PhD, School of Computer Science and Engineering, University of New South Wales (UNSW), Sydney -2052, Australia, 2001. Area of research: formal methods in software engineering.
- M.Tech in Computer and Information Tech., Indian Institute of Technology, Kharagpur, 1994.
- B.E in Computer Science and Engineering, College of Engineering, Anna University Madras, 1989.

**Professional Experience:**

1. 2013 December: Associate Professor.
2. 2013: Adjunct Professor, Indian Institute of Technology, Kanpur.
3. 2010 January - continuing: Program Director of Computer System Engineering, Department of Electrical & Computer Engineering (ECE), University of Auckland. I am responsible for overseeing the curriculum delivery and administration of the Computer Systems Engineering program in ECE.
4. 2009 January - 2009 June: Visiting Professor, Christian-Albrechts-University Kiel, Germany with a fellowship for experienced researchers from the Alexander von Humboldt Foundation, Germany.
5. 2009 January - continuing: Senior Lecturer over the proficiency bar, Department of Electrical & Computer Engineering, University of Auckland.
6. 2003 September-2008 December: Senior Lecturer, Department of Electrical & Computer Engineering, University of Auckland. Responsible for teaching and research inn the area of *Computer Systems Engineering* where students specialize in embedded systems after two years of common with conventional Electrical Engineering program.
7. 2001 January-2003 August: Lecturer, Department of Electrical and Electronic Engineering, University of Auckland, New Zealand. Responsible for teaching and research in the areas of *embedded systems* and *software engineering*.

8. 1997-2000: Full-time PhD Student, School of CSE, UNSW, Sydney, Australia from March 1997 to October 2000. Developed a method which can automatically reuse embedded components from a library of components during the design synthesis of *embedded systems*. Given the time-to-market pressures and increasing system complexities, *component reuse* during synthesis is being touted as a key to success. This research formulated and implemented a *polynomial-time algorithm* for reusing components from the component library.

9. 1999-2000: Associate Lecturer (part-time), School of CSE, UNSW, Australia. Administered one post-graduate software engineering course and an under-graduate data organization course. The responsibilities included regular student consultations, tutorials, test suits for automatic testing of assignments, creating and maintaining student databases, creating and maintaining subject web-pages, evaluating examination scripts.

10. 1995-1997: Assistant Professor of Computer Science, Regional Engineering College (REC) [Now National Institute of Technology], Rourkela, India from December 1995 to January 1997. In addition to teaching and administrative responsibilities, pursued collaborative research with colleagues at Indian Institute of Technology, Kharagpur to develop hardware-software codesign tools for embedded systems. This resulted in two major publications including one in the IEEE transactions. Also developed some interesting query optimization technique for indefinite databases with colleagues at REC, Rourkela.

11. 1990-1995: Lecturer, Regional Engineering College [Now National Institute of Technology], Rourkela, India from July 1990 to December 1995. Taught and developed course material for several courses offered by the school, including Computer Architecture, Computer Organization and Design, Artificial Intelligence, Databases, Operating Systems. Also worked on extending relational databases to handle indefinite information and developed a new join operator for such databases. New techniques for automatic protocol matching were also proposed during this period.

**Significant Distinctions / Awards**

1. 2015, Mercator Fellowship (professorship), German Science Foundation (DFG), March - November 2016.

2. 2014, French National Laboratory for Informatics and Control (INRIA), Visiting Professor Fellowship, November 2014.

3. 2013, Best paper award, ACM International Conference on Compilers, Architecture, and Synthesis for Embedded Systems (CASES), Embedded Systems Week, October 2013. [USD 500 cash prize; top conference in embedded systems].

4. 2011, Invited Speaker, World Congress on Intelligent Transportation Systems (ITS), Orlando, Florida. [chaired a panel on vehicles of the future with Jeffrey Spencer (Head of Intelligent Transportation Systems, Department of Transport, USA), Robyn North (Imperial College) and Steve Novosad (President of ITS, Texas)].

5. 2011, Invited Speaker, 11th Asia Pacific Intelligent Transportation System (ITS) Forum, Kaohsiung, Taiwan.
6. 2011, Short listed for the submission of teaching profile for faculty teaching award (excellence in supervision category).
7. 2010, Top fifteen faculty teachers award, Faculty of Engineering, University of Auckland.
8. 2009, Alexander von Humboldt Foundation fellowship for Experienced Researchers, Germany.
9. 2008, Host for Marie Curie International Research Fellow, Dr. Alain Girault, INRIA, Rhone-Alpes, France.
10. 2007, Visiting Professor Award, INRIA, Rhone-Alpes, France.
11. 2006, Best Paper Award, Foundations of Embedded Software and Component-Based Software Architectures (FESCA 2006), Vienna, Austria, March 2006.
12. 2005, Top 20 Faculty Teacher Award, Faculty of Engineering, University of Auckland.
13. 2004, Top 20 Faculty Teacher Award, Faculty of Engineering, University of Auckland.
14. 2002, Early Career Research Award, University of Auckland.
15. 2000, Best Paper Nomination in 2000 VLSI Design Conference.
16. 1996, Australian Development Cooperation Scholarship, AUSAID, All India Rank 2nd.
17. 1993, 2nd Top Student in ME (Computer Science), Indian Institute of Technology, Kharagpur.

**Professional Activities:**

1. Member of New Zealand Review Group, ISO Technical Committee 204.
2. Program Co-chair, 19 IEEE International Symposium on Real-Time Computing, York, UK, May 2016.
3. General Chair, 18th IEEE International Symposium on Real-Time Computing, Auckland, April 2015.
4. TPC Member, IEEE Real-Time and Embedded Technology and Applications Symposium (RTAS 2015).
5. TPC Member, ACM International Conference on Embedded Software (EMSOFT), 2015.
6. Co-opted board member (until July 2012) of Intelligent Transportation Systems (ITS), New Zealand (www.itsnz.org.nz). This is a national body responsible for ITS policies in NZ and also interacts with other national-level ITS bodies in the world.
7. Associate Editor, Elsevier journal of Microprocessors and Microsystems (MICPRO).

8. Associate Editor, Springer/EURASIP journal of Embedded Systems.

**Service to the University:**

1. Program Director of the Computer Systems Engineering program from 2010-2015.
2. Led the preparation of portfolio and appendices for the department review 2015.
3. Selection committee for CSE Lecturer / Senior Lecturer appointments 2015.

**Recent Publications / Patents:**

Patents:

1. S. A. Ali, Z. Bhatti, P. S. Roop, "Automatic process and system for software development kit for application programming interfaces", PCT/NZ2015/000019, March 2015.
2. P. S. Roop and A Malik, System and Method for emulating hybrid systems", NZ Provisional Patent Application 711839 (submitted).

Books:

1. Li Hsien Yoong, Partha S Roop, Zeeshan Bhatti and Matthew Kuo, "A Synchronous Approach for Embedded and Automation Systems", Springer, 2015.
2. Roopak Sinha, Partha S Roop and Samik Basu, "Correct by construction approaches for System on a Chip (SoC) Design", Springer, 2013.

Refereed Journals:

1. R. Sinha, P. S. Roop, G. Shaw, Z. Salcic, M. Kuo, "Hierarchical and Concurrent ECCs for IEC 61499 Function Blocks", IEEE Transactions on Industrial Informatics, To appear (accepted).
2. Sidharta Andalam, Partha S Roop, Alain Girault, Claus Traulsen, "A Predictable Framework for Safety-Critical Embedded Systems," IEEE Transactions on Computers, vol. 63, no. 7, pp. 1600-1612, July, 2014
3. Sinha, R., Girault, A., Goessler, G., & Roop, P. S. (2014). A Formal Approach to Incremental Converter Synthesis for System-on-Chip Design. ACM Transactions on Design Automation of Electronic Systems (TODAES), 20(1), 13.
4. Reinhard von Hanxleden and Michael Mendler and Joaqun Aguado and Bjrn Duderstadt and Insa Fuhrmann and Christian Motika and Stephen Mercer and Owen OBrien and Partha Roop. "Sequentially Constructive Concurrency–A Conservative Extension of the Synchronous Model of Computation". ACM Transactions on Embedded Computing Systems, Special Issue on Applications of Concurrency to System Design, 13(4s):144:1144:26, 2014.
5. R. Sinha, P. S. Roop and P. Ranjitkar, "Virtual traffic lights+: A robust, practical and functionally safe intelligent transportation system", Transportation research records, Volume 2381, pp. 73-80, February 2013, ISSN: 0361-1981.

6. S. A. Ali, P. S. Roop and I. Warren, Web service choreography: unanimous handling of control and data, International Journal of Software and Informatics, 7(2), pp. 309-330, 2013.
7. L. H. Yoong and G. D. Shaw and P. S. Roop, Z. Salcic, " Synthesizing Globally Asynchronous Locally Synchronous Systems With IEC 61499", IEEE Transactions on Systems, Man, and Cybernetics–Part C: Applications and Reviews, 42(6), pp. 1465-1477, 2012.
8. L. H. Yoong and P. S. Roop, Z. Salcic, "Implementing Constrained Cyber-Physical Systems with IEC 61499", ACM Transactions in Embedded Computing Systems (TECS), 11(4), 2012.
9. L. H. Yoong and P. S. Roop, "Verifying IEC 61499 Function Blocks Using Esterel", IEEE Embedded Systems Letters, Vol. 2, No.1, March 2010
10. A. Malik, Z. Salcic, P. S. Roop and A. Girault, "SystemJ: A GALS Language for system Level Design", 36(4), December 2010, Elsevier Journal on Computer Languages.
11. I. Radojevic, Z. Salcic and P. S. Roop, "Design of distributed heterogeneous embedded systems in DDFCharts", IEEE Transactions on parallel and distributed systems, 22(2), 2010, 14 pages.
12. L. H. Yoong, P. S. Roop, V. Vyatkin, Z. Salcic, "A synchronous approach for IEC61499 Function Block Implementation", IEEE Transaction on Computers, 58(12), pp. 1599-1614, 2009.
13. Avinash Malik, Zoran Salcic and P. S. Roop, "SystemJ Compilation using the Tandem Virtual Machine Approach", ACM Transactions on the Design Automation of Electronic Systems (TODAES), 14(3), pp. 1-37, May 2009.
14. Simon Yuan, Li Hsien Yoong, Sidharta Andalam, P. S. Roop, Zoran Salcic, "A new multithreaded architecture supporting direct execution of Esterel", EURASIP Journal of Embedded Systems, Volume 2009 (2009), Article ID 610891, 19 pages, doi:10.1155/2009/610891.
15. R. Sinha, P. S. Roop, S. Basu, "SoC design approach using Convertibility Verification", EURASIP Journal on Embedded Systems, Volume 2008 (2008), Article ID 296206, 19 pages, doi:10.1155/2008/296206.
16. V. Vyatkin, Z. Salcic, P. S. Roop and J. Fitzgerald, "Information Infrastructure of Intelligent Machines based on IEC61499 Architecture", IEEE Industrial Electronics Magazine, 1(4): 17-29, 2007.
17. H.-F. Guo, M. Liu, P. S. Roop, C. R. Ramakrishnan and I. V. Ramakrishnan, "Precise specification matching for adaptive reuse in embedded systems", Journal of Applied Logic,5(2): 333-355, 2007.
18. I. Radojevic, Z. Salcic and P. S. Roop, "Modelling Heterogeneous Embedded Systems: From SystemC and Esterel to DFCharts", IEEE Design and Test of Computers, 23(5): 348-357, 2006.
19. Z. Salcic, D. Hui, P. S. Roop and M. Biglari-Abhari, "HiDRA - A reactive microprocessor architecture for Heterogeneous Embedded Systems", Elsevier Journal of Microprocessors and Microsystems, 30(2): 72-85, 2006.

20. I. Radojevic, Z. Salcic and P. S. Roop, "A New Model for Heterogeneous Embedded Systems", International Journal of Software Engineering and Knowledge Engineering, 15 (2): 405-410, 2005.
21. P. S. Roop, A. Sowmya, S. Ramesh, Haifeng Guo, "Tabled Logic Programming Based IP Matching Tool using Forced Simulation", IEE Proceedings on Computer and Digital Techniques, 151(3): 199-208, 2004.
22. Z. Salcic, P. S. Roop, M. Biglari-Abhari, A. Bigdeli, "REFLIX: A Processor Core with Native Support for Control Dominated Embedded Applications", Elsevier Journal of Microprocessors and Microsystems, 28(1): 13-25, 2004.
23. P. S. Roop, A. Sowmya, S. Ramesh, "Forced Simulation: A Technique for Automating Component Reuse in Embedded Systems", ACM Transactions on Design Automation of Electronic Systems, 6(4): 602-628, 2001.
24. R. S. Mitra, P. S. Roop, and A. Basu, "A new algorithm for the implementation of design functions by available devices", IEEE Transactions on very large scale integration (VLSI) systems, 4(2):170-180, June 1996.
25. R. S. Mitra, P. S. Roop, and A. Basu, "An overview of Micky - A knowledge based hardware-software codesign framework for microprocessor based systems", Sadhana-Academy Proceedings in Engineering Sciences. 21(6): 719-739, 1996.

Book Chapters/ Electronic Notes:

1. Yu Zhao and Partha S Roop, "Model driven design of a cardiac pacemaker using IEC61499", chapter in Distributed Control Applications: Guidelines, Design Patterns, and Application Examples with the IEC 61499, CRC Press, 2015.
2. Matthew M Y Kuo and Partha S Roop, "New design patterns for time predictable execution of function blocks", chapter in Distributed Control Applications: Guidelines, Design Patterns, and Application Examples with the IEC 61499, CRC Press, 2015.
3. Zachary J. Oster, Syed Adeel Ali, Ganesh Ram Santhanam, Samik Basu, and Partha S Roop, "A Service Composition Framework Based on Goal-Oriented Requirements Engineering, Model Checking, and Qualitative Preference Analysis", 10 International Conference on Service Oriented Computing, Shanghai, China, November 2012 (accepted 32 out of 185 submissions).
4. Simon Yuan, Sidharta Andalam, Li Hsien Yoong, Partha S. Roop, Zoran A. Salcic, "STARPro - A new multithreaded direct execution platform for Esterel", Electr. Notes Theor. Comput. Sci. 238(1): 37-55 (2009).
5. Roopak Sinha, Partha S. Roop, Samik Basu, "A Model Checking Approach to Protocol Conversion", Electr. Notes Theor. Comput. Sci. 203(4): 81-94 (2008).
6. Samik Basu, Partha S. Roop, Roopak Sinha, "Local Module Checking for CTL Specifications", Electr. Notes Theor. Comput. Sci. 176(2): 125-141 (2007). [Best Paper Award]
7. Reinhard von Hanxleden and Xin Li and Partha S Roop and Zoran Salcic and Li Hsien Yoong. "Reactive Processing for Reactive Systems". ERCIM News, (66):2829, 2006.

8. Robi Malik and Partha S. Roop, "Adaptive Techniques for Specification Matching in Embedded Systems: A Comparative Study", Lecture Notes in Computer Science, 2005, Volume 3771, 2005, 33-52, 33-52.
9. Roopak Sinha, Partha S. Roop, Bakhadyr Khoussainov, "Adaptive Verification using Forced Simulation", Electr. Notes Theor. Comput. Sci. 141(3): 171-197 (2005).
10. Z. Salcic, P. S. Roop, M. Biglari-Abhari, A. Bigdeli, "REFLIX: A Processor Core for Reactive Embedded Applications", 12th International Conference on Filed Programmable Logic and Applications, LNCS 2438: 239-267, Montpellier, France, 2002.

Refereed Conferences:[1].

1. *Nathan Allen, Sidharta Andalam, Partha S Roop, Avinash Malik, Mark Trew, Nitish Patel, "Modular code generation for emulating the electrical conduction system of the human heart", Design Automation and Test in Europe (DATE), March 2016, Dresden, Germany (accepted as a full paper).
2. *Matthew Kuo, Sidharta Andalam, Partha S Roop, "Precision Timed Industrial Automation Systems", Design Automation and Test in Europe (DATE), March 2016, Dresden, Germany (accepted as full paper).
3. *Weiwei Ai, Nitish Patel, Partha S Roop, "Requirements-centric closed loop validation of implantable cardiac devices", Design Automation and Test in Europe, March 2016, Dresden, Germany (accepted as an interactive presentation).
4. *Li Hsien Yoong and Partha S Roop, "Synthesizing Multirate Programs from IEC 61499", 18th International Symposium on Real-Time Computing (ISORC), Auckland, 13-17 April 2015.
5. *Jin Woo Ro, Partha S Roop, Avinash Malik, Schedule synthesis for time-triggered multi-hop wireless networks with retransmissions, 18th International Symposium on Real-Time Computing (ISORC), Auckland, 13-17 April 2015.
6. *Mahmood Hikmet, Partha S Roop, Prakash Ranjitkar, "Fairness-Based Measures for Safety-Critical Vehicular Ad-Hoc Networks", 18th International Symposium on Real-Time Computing (ISORC), Auckland, 13-17 April 2015.
7. Hammond Perace, Roopak Sinha, Partha S. Roop, "An Augmented Reality Demo Environment for ITS Systems", 13th Asia Pacific ITS Forum, Auckland, New Zealand, April 2014.
8. *Jin Woo Ro, Zeeshan E. Bhatti and Partha S. Roop, "A model-driven approach with synchronous semantics for developing hard real-time WSNs", 19th IEEE International Conference on Emerging Technologies in Factory Automation (ETFA), Barcelona, Spain, September 2014.
9. *Eugene Yip, Matthew Kuo, Partha S. Roop and David Broman, "Relaxing the Synchronous Approach for Mixed-Criticality Systems", 20th IEEE Real-Time and Embedded Technology and Applications Symposium (RTAS), Berlin, Germany 2014.

[1] **I have marked conference papers with acceptance rates of 20-40% of archival value as ***

10. Michael Mendler, Bruno Bodin, Partha S. Roop, and Jai Jie Wang, "The WCRT analysis of synchronous programs: Studying the tick alignment problem", RePP workshop, Grenoble, France, 2014.

11. *J. Wang, P. S. Roop and S. Andalam, "ILPc: A novel approach for scalable timing analysis of synchronous programs", International Conference on Compilers, Architecture, and Synthesis for Embedded Systems (CASES), ACM, October 2013. [**Best paper award**]

12. Roopak Sinha, Partha S Roop, Prakash Ranjitkar, Junbo Zeng, Xingchen Zhu " Model-based Design of Coordinated Traffic Controllers", 20th ITS World Congress, Tokyo, Japan, 14-18 October 2013.

13. *Syed Adeel Ali, Partha S Roop and Ian Warren, "Stateful Web Services - Auto Modeling and Composition", 20th IEEE International Conference on Web Services (ICWS 2013), June 27-July 2, 2013, Santa Clara Marriott, CA, USA.

14. *Eugene Yip, Partha S Roop, Morteza Biglari-Abhari, Alain Girault, "Programming and Timing Analysis of Parallel Programs on Multicores", 13th International Conference on Application of Concurrency to System Design, June 8-July 10 2013.

15. *Matthew Kuo, Partha S Roop, Sidharta Andalam and Nitish Patel, "Precision Timed Embedded Systems Using TickPAD Memory", 13th International Conference on Application of Concurrency to System Design, June 8-July 10 2013.

16. *S. Andalam, R. Sinha, P. S. Roop, A. Girault and J. Reineke, "Precise Timing Analysis of Direct Mapped Caches", Design Automation Conference (DAC), 2013.

17. *M. Kuo, P. S. Roop and N. D. Patel, "Precision Timed Systems Using TickPAD Memory", Design Automation Conference (DAC), 2013 (accepted as a WIP presentation).

18. J. Wang, P. S. Roop and S. Andalam, "ILPc: A novel approach for scalable timing analysis of synchronous programs", Design Automation Conference (DAC), 2013 (accepted as a WIP presentation).

19. Roopak Sinha, Partha S Roop, Prakash Ranjitkar, "Virtual Traffic Lights+ (VTL+): A Robust, Practical, and Functionally-Safe Intelligent Transportation System", in proc. Transportation Research Board, 92 Annual Meeting, Washington DC, January 2013.

20. Li Hsien Yoong, Zeeshan Bhatti and Partha S Roop, "Combining IEC 61499 Model-Based Design with Component-Based Architecture for Robotics", SIMPAR 2012, to be held in Tsukuba, Japan, during November 5-8, 2012, proceedings will be published by Springer as a book in the LNCS series.

21. Kyle Nicholas, Zeeshan Bhatti and Partha S Roop, "Model-Driven Development of Industrial Embedded Systems : Challenges Faced and Lessons Learnt", 17th IEEE International Conference on Emerging Technologies and Factory Automation (ETFA), September, Poland, 2011.

22. *Roopak Sinha, Partha S Roop, Zoran Salcic and Samik Basu, "Correct-by-construction Multi-component SoC Design", Design Automation and Test in Europe (DATE), Dresden, Germany, IEEE Computer Society, 2012.

23. Simon Yuan, Li Hsien Yoong and Partha S Roop, "Compiling Esterel for Multi-core Execution", 14th *EUROMICO Digital System Design, August 31-Spetember 2, Oulu, Finland, 2011.
24. Zeeshan Bhatti, Roopak Sinha and Partha S Roop, "Observer based verification of IEC61499 Function Blocks", IEEE International Conference on Industrial Informatics, Caparica, Lisbon, Portugal from 26th June to 29th July 2011.
25. Bruce MacDonald, Partha S Roop, Tanveer Abbas, Chandimal Jayawardena, Chandan Datta, Jamie Diprose, John Hosking, Zeeshan Bhatti, "Case studies for model driven engineering in mobile robotics", 6th workshop on Software Development and Integration in Robotics, ICRA Workshop, Shanghai, China, May 2011.
26. *M. Kuo, R. Sinha, P. S. Roop, "Efficient WCRT Analysis of Synchronous Programs using Reachability", ACM Design Automation Conference (DAC), San Diego, June 2011.
27. *S. Andalam, P. S. Roop, A. Girault, "Pruning Infeasible Paths for Tight Timing Analysis of Synchronous Programs". Proceedings of Design Automation and Test in Europe (DATE), March, 2011.
28. S. Andalam, R. Sinha and P. S. Roop, Environment Modelling for Tight Timing Analysis of Synchronous Programs. The 6th International Symposium on Electronic Design, Test and Applications (DELTA), January, 2011.
29. *Andalam, P. S. Roop, A. Girault, "Predictable multithreading of embedded applications using PRET-C". Proceedings of ACM-IEEE International Conference on Formal Methods and Models for Codesign (MEMOCODE), 2010.
30. Matthew M Y Kuo, Li Hsien Yoong, Sidharta Andalam, and Partha S Roop, "Determining the Worst-Case Reaction Time of IEC 61499 Function Blocks", 8th IEEE International Conference on Industrial Informatics, July 130-16, Osaka, Japan, 2010.
31. Gareth D. Shaw, Partha S. Roop and Zoran Salcic, "Reengineering of IEC 61131 into IEC 61499 Function Blocks", 8th IEEE International Conference on Industrial Informatics, July 130-16, Osaka, Japan, 2010.
32. *S. Andalam, P. S. Roop, A. Girault, "Deterministic, predictable and light-weight multithreading using PRET-C", in proc. Design Automation and Test in Europe (DATE), 2010.
33. S. Andalam, P. S. Roop, A. Girault, and C. Traulsen, "PRET-C: A new language for programming precision timed architectures", in the Workshop on Reconciling Performance with Predictability (RePP), Embedded Systems Week, Grenoble, France, 15 October 2009.
34. *P. S. Roop, S. Andalam, R von Hanxleden, S. Yuan, C. Traulsen, "Tight WCRT analysis of synchronous C programs", ACM International conference on compilers, architectures and synthesis of embedded systems (CASES), October 11-16, Grenoble, France, 2009.
35. *Gareth D. Shaw, Partha S. Roop, Zoran Salcic, "A hierarchical and concurrent approach for IEC 61499 function blocks", IEEE International Conference on Emerging Technologies and Factory Automation (ETFA), September 22-26, Spain, 2009.

36. *P. S. Roop, A. Girault, R. Sinha and G. Goessler, "Specification enforcing refinement using convertibility verification", 9th International Conference on Application of Concurrency to System Design 2009 to be held in Augsburg, Germany, 1-3 July 2009.
37. Gareth Shaw, Li Hsien Yoong, Partha S Roop and Zoran Salcic, "Model-driven Approach for Complex Material Handling Systems", 13th IFAC Symposium on Information Control Problems in Manufacturing (INCOM '09) to be held at Institute of Moscow, Russia, June 3-5, 2009.
38. *R. Sinha, P. S. Roop, S. Basu and Z. Salcic, "Multi-Clock SoC Design using Protocol Conversion", Design Automation and Test in Europe (DATE), Nice France, April 2009.
39. L. H. Yoong, P. S. Roop, and Z. Salcic, "Efficient implementation of IEC 61499 function blocks", in IEEE International Conference on Industrial Technology (ICIT), Gippsland, February 2009.
40. A. Malik, Z. Salcic and P. S. Roop, "Tandem virtual machine An efficient execution platform for GALS language SystemJ", Computer Systems Architecture Conference, 2008. ACSAC 2008. 13th Asia-Pacific , vol., no., pp.1-8, 4-6 Aug. 2008
41. *Roopak Sinha, Partha S Roop and Samik Basu and Zoran Salcic, "A Module Checking based Converter Synthesis Approach for SOCs", IEEE International Conference on VLSI Design, 4th to 8th January 2008, Hyderabad, India.
42. *Ivan Radojevic, Zoran Salcic and Partha S Roop, "McCharts and Multiclock FSMs for Modelling Large Scale Systems", Fifth ACM-IEEE International Conference on Formal Methods and Models for Codesign (MEMOCODE'2007), pp. 3-12, May 30 - June 1st, Nice, France, 2007.
43. R. Sinha, P. S. Roop and S. Basu, "A Model Checking Approach to Protocol Conversion", in proc. Model Driven high-Level Programming of Embedded Systems (SLA++P), European Joint Conference on Theory and Practice of Software, Braga, Portugal, ENTCS 176(2): 125-141, 2007.
44. Li Hsien Yoong, Partha S Roop and Zoran Salcic and V. Vyatkin, "Synchronous execution of IEC61499 Function Blocks using Esterel", 5th IEEE International Conference on Industrial Informatics, 2: 1189-1194, July 23rd-27th, Vienna, Austria, 2007.
45. *Z. Salcic, F. Gruian, P. S. Roop and A. Wahid, "A Scheduler support Unit for Reactive Microprocessors", The 12th IEEE International Conference on Embedded and Real-Time Computing Systems and Applications, pp. 368-372, Sydney, Australia, 2006.
46. *F. Gruian, P. S. Roop, Z. Salcic and I. Radojevic, "The SystemJ Approach to system Level Design", Fourth International Conference on Formal Methods and Models for Codesign, MEMOCODE 2006: 149-158, Napa, California, July 2006.
47. Li Hsien Yoong, Partha S Roop and Zoran Salcic, "Compiling Esterel for Distributed Execution", in proc. Synchronous Languages, Applications and Programming 2006, European Joint Conference on Theory and Practice of Software, March 25- April 2, Vienna, Austria, 2006 (to appear in ENTCS).

48. *Ivan Radojevic, Zoran Salcic, Partha S. Roop, "Design of Heterogeneous Embedded Systems Using DFCharts Model of Computation", Proceedings of VLSI Design 2006: 461-464, January 3- 7, 2006, Hyderabad, India.

49. Ivan Radojevic, Zoran Salcic, Partha S. Roop, "Modeling Heterogeneous Embedded Systems in DFCharts", Proceedings of Forum on Design and Specification Languages (FDL), September 27- 30, 2005, Lausanne, Switzerland.

50. M.W. Sajeewa Dayaratne, P. S. Roop, Z. Salcic, "Direct Execution of Esterel Using Reactive Microprocessors", in proc. Synchronous Languages, Applications, and Programming, April 3rd, 2005, Edinburgh, Scotland (to appear in ENTCS).

51. *Z. Salcic, D. Hui, P. S. Roop and M. Biglari-Abhari, "REMIC - Design of a Reactive Embedded Microprocessor Core", Design Automation Conference, Proceedings of the 10th Asia and South Pacific Design Automation Conference, ASP-DAC 2005: 977-981, China, 18-21 January, 2005.

52. *P. S. Roop, Z. Salcic, M. W. S. Dayaratne, "Towards Direct Execution of Esterel Programs on Reactive Processors", 4th ACM International Conference on Embedded Software, EMSOFT 04:240-248, Pisa, Italy, September 27-29, 2004.

53. Z. Salcic, P. S. Roop, "Customizing Processor Cores to Support Reactivity", The 2004 International Conference on Engineering Reconfigurable Systems and Algorithms, ERSA 2004:194-202, Las Vegas, June 21-24, 2004.

54. Z. Salcic, P. S. Roop, D. Hui, I. Radojevic, "HiDRA: A New Architecture for Heterogeneous Embedded Systems", the 2004 International Conference on Embedded Systems and Applications, ESA/VLSI 2004: 164-170, Las Vegas, June 21-24, 2004.

55. *P. S. Roop, Z. Salcic, M. Biglari-Abhari, A. Bigdeli, "A New Reactive Processor with Architecture Support for Control Dominated Embedded Systems", IEEE International Conference on VLSI Design, VLSI Design 2003: 189-194, IEEE CS Press, pp.189-194, 2003.

56. R. Mugridge, B. MacDonald, P. S. Roop, "A Customer Test Generator for Web based systems", the fourth International Conference on eXtreme Programming and Agile Processes in Software Engineering, XP 2003: 189-197, Genova, Italy, (LNCS Series).

57. R. Mugridge, B. MacDonald, P. S. Roop, E. Tempero, "Five Challenges in Teaching XP", Educational Symposium, Fourth International Conference on eXtreme Programming, XP 2003: 406-409, Genova, Italy.

58. *P. S. Roop, A. Sowmya, S. Ramesh,, "k-time Forced Simulation: A Formal Verification Technique for IP Reuse", IEEE International Conference on Computer Design, ICCD 2002: 50-56, Freiburg, Germany, 2002.

59. *P. S. Roop, A. Sowmya, S. Ramesh, "Component based development of synchronous programs", Asia Pacific Design Automation Conference, Yokohama, January 2001 (IEEE Computer Society).

60. *P. S. Roop, A. Sowmya, S. Ramesh, "Automatic Component Matching using Forced Simulation", 13th International Conference on VLSI Design, January 2000, IEEE Computer Society. [Best Paper Award Nominee]

61. P. S. Roop, A. Sowmya, S. Ramesh "Automated component adaptation by forced simulation", Proc 5th Australasian Computer Architecture Conference, Australian Computer Science Communications, Vol. 22, No.4, Eds. G. Heiser, Canberra Australia, 31-3 Jan. 2000, IEEE Computer Science Society, Los Alamitos, California, 2000, pp74-81.
62. D. Castra, P. S. Roop and A. Sowmya, "Compiling CFSMcharts specifications to ESTEREL", in proc. of 6th Australasian Conf. on Parallel and Real-Time Systems ' 99, Eds. Wilson C. H.Cheng; A. S. M. Sajeev, Melbourne, Australia, 29-1 Nov. 1999, Springer Verlag, Singapore, 1999, pp298-30.
63. P. S. Roop, A. Sowmya A, G. C. Mormanis, S. S. Baldwin, "Application of CFSMcharts for modelling real-time and industrial embedded systems", Proceedings of 15th IFAC Workshop Distributed Computer Control Systems, Eds. F. De Paoli; I. M. MacLeod, Como Italy, 9-11 Sep. 1998, Elsevier science, Oxford, U. K., 1998, pp93-100.
64. *P. S. Roop, and A. Sowmya, "CFSMcharts: A New Language for Microprocessor Based System Design", in Proc. 11th International Conference on VLSI Design: 342-346, IEEE Computer Society, pp. 342-346, January 1998, Chennai, India.
65. *P. S. Roop, and A. Sowmya, "Hidden Time Model for the Specification and Verification of Embedded Systems", the 10th Euromicro Workshop on Real-Time Systems, Euromicro RTS:98-105, IEEE Computer Society Press, June 17th-19th, Berlin, Germany.
66. P. S. Roop, and A. Sowmya, "Functional Decomposition of Composite Finite State Machines", In Proc. of the 4th Annual Australasian Conference on Parallel and Real-Time Systems (PART'97), Springer Verlag, pp. 422-433, 29th - 30th Sept., New castle, Australia.
67. P. S. Roop, C. V. Sastry, R. S. Raghavan and A. Basu, "A new algorithm for mapping a design function to multiple devices", in proc. of the 3rd APCHDL 1996.
68. *R. S. Mitra, P. S. Roop, and A. Basu, "Implementation of Design Functions by Available Devices: A New Algorithm", in Proc. of IEEE International Conference on VLSI Design, VLSI 1995: 170-180, , New Delhi, Jan. 1995.
69. R. S. Mitra, P. S. Roop, and A. Basu, "A Multilayer Design Expert System with Resilience", in Proc. of 3rd IEEE Symp. On Intelligent Systems, Bangalore, pp. 128- 134, Nov. 1993.
70. P. K. Bhutia, P. S. Roop, C. V. Sastry., "Query Optimization in Indefinite Databases", CISMOD'92, Bangalore, India: Indian National Scientific Documentation Centre, 1992.

**Technical Reports:**

1. A. Malik, P. S. Roop, S. Andalam, E. Yip, M. Trew, "A synchronous rendering of hybrid systems for designing plant on a chip", Technical Report, Cornell University, arXiv:1510.04336, October 2015. **This paper is under review in IEEE transactions on software engineering (TSE)**.

2. A. Malik, P. S. Roop, "A unified framework for modeling and implementation of hybrid systems with synchronous controllers", Technical Report, Cornell University, arXiv:1501.05936, 2014.

3. M. Mendler, B. Bodin, P. S. Roop and J. J. Wang, "WCRT of synchronous programs: studying the tick alignment problem", Technical Report No. 95, August 2014, ISSN 0937-3349, Bamberg University, Germany.

4. S. Yuan, L. H. Yoong and lineP. S. Roop, "Efficient compilation of Esterel for Multi-core execution", Technical Report No. 8056, INRIA Grenoble Rhone-Alpes, 2012.

5. S. Andalam, P. S. Roop, A. Girault, and C. Traulsen, "PRET-C: A new language for programming precision timed architectures" Technical Report 6922, INRIA Grenoble Rhone-Alpes, 2009.

6. Partha S Roop, Sidharta Andalam, Reinhard von Hanxleden and Simon Yuan and Claus Traulsen,"Tight WCRT analysis of synchronous C Programs", Technical Report No. 0912, Christian-Albrechts-Universitat Kiel, Department of Computer Science, May 2009.

7. P. S. Roop, "Predictable Reactive Processors for Next Generation Computing: A Proposal", Report 662, School of Engineering, University of Auckland, 2008.

8. R. Sinha, P. S. Roop and S. Basu, "An Approach for Resolving Control and Data Mismatches in SoCs". Report 667, School of Engineering, University of Auckland, 2008.

9. R. Sinha, P. S. Roop and S. Basu, "A Model Checking based Converter Synthesis Approach for Embedded Systems", Iowa State University Technical Report No. 537, 2006.

10. Partha S Roop, A. Sowmya and S. Ramesh, "Forced Simulation: A Formal Approach-to Component-Based Synthesis", UNSW, School of CSE Tech. Rep. No. UNSW-CSE-TR-9901, March 1999.

11. Partha S Roop, A. Sowmya and S. Ramesh, "Forced Simulation and Lock-Step Ininterface: A Formal Approach to Automatic Component Matching", UNSW, School of CSE Tech. Rep. No. UNSW-CSE-TR-9903, June 1999.

**Commercialization:**

1. Cloud services spin-out: I have successfully commercialized my research as a venture company called APIMatic (apimatic.io) which is a leading provider of automatic SDK generation software on many platforms. ApiMatic has received venture funding of $417K (2014) and US$600K (2015).

2. Minimum viable product (MVP) on Internet of things (IoT): UniServices has funded $80k in 2015 to prepare an MVP in the area of IoT. The proposed company, called IoTa (Internet of things and applications) is developing a web-based software that will significantly reduce the design and prototyping effort in this domain and significantly reduce the time to market.

3. BlokTech: This was a spin-out for model driven development of industrial automation software. While the company was unsuccessful, the technology is available for use (timeme.io) and is listed on the web-pages of the international standard: (www.iec61499.de/tools.htm).

**Research/commercialization Funding:**

- P. S. Roop, Mercator Fellowship, **Precision Timed Synchronous Reactive Processing**, German Science Foundation(DFG), EUR 71, 000.
- P. S. Roop, **The IoTa tool-kit for Internet of things**, Uniservices Commercialization Grant, $80,000, 2015.
- P. S. Roop, M. Trew, A. Malik, **Heart-on-FPGA: Taming arrhythmia through timing models of the heart**, $158,412, FRDF grant, University of Auckland (funding for a Postdoctoral fellow for 2 years).
- P. S. Roop, Adeel Ali and Zeeshan Bhatti (PIs), **APIMatic**, Venture Capital Funding from SparkBox and other venture funds, $357, 000, April 2014.
- P. S. Roop (PI), **APIMatic - toolkit for seamless APIs reuse in the cloud**, UniServices Stage-gate fund, $60,000, Dec 2013.
- P. S. Roop (PI), **Safety-Critical Robotics**, Research Capex, NZD 16, 960, 2012.
- P. S. Roop (PI), **Real-Time Networking for Innovative Manufacturing**, Research Capex, $43,979, 2011.
- P. S. Roop (PI) and P. Ranjitkar (AI), **Functional safety of intelligent transportation**, $134, 500, 2011.
- PIs–M. Mendler, R von Hanxleden (Germany) , External Collaborators–E. A. Lee (UC Berkeley), S. A. Edwards (Columbia) and R. Wilhelm (Saarland), P. S. Roop (Auckland), **Precision Timed Synchronous Processing**, EUR 473,000, DFG, November 2011.
- P. S. Roop, PI, **Model Driven Engineering**, MSI Capability Education Grant with Tru Test Ltd, $36,000, 2011.
- P. S. Roop, V. Vyatkin, Co-PI, **BlokTech Systems**, Trans Tasman Commercialization fund and Spark-Box Ltd, $350K, 2010.
- Alain Girault et al. from INRIA, France; Z. Salcic and P. S. Roop from UoA **Advanced Formal Methods for Embedded Systems**, Associated Team Proposal, 2010, EUR50,000.
- P. S. Roop, PI, **TimeMe - A New Design Methodology for Safety-Critical Systems**, Auckland UniServices Stage-Gate Grant, 2010, $60,000, 2010.
- P. S. Roop and V. Vyatkin, Co-PI, **Function Block Systems**, Auckland UniServices Stage-Gate Grant, 2010, $140,000, 2010.

- V. Vyatkin (PI) and P. S. Roop (AI), NSF FREEDM Project, USD 50,000.
- B. MacDonald (PI), P. S. Roop and others (AI), VC's IRTDA Grant, $60,000 per year, 2010.
- P. S. Roop, **INRIA Visiting Professor Grants and additional support for SYNCHRON**, 2007, 2009, 2012, 2014 approx. $ 30,000.
- P. S. Roop, PI, **The Design of Augmented Reality Sports Environments**, Faculty Research Development Fund Post Doc Grant, October 2009-October 2011, $68,000.
- Ross Green et al. (from Wellington Drives Ltd), Z. Salcic, P. S. Roop et al. from UoA, Technology for Business Growth grant from Foundation for Research Science and Technology, New Zealand, Approx: 4.6 million NZD [University share $9,00,000].
- Marie Curie Fellow – Alain Girault, Hosts – P. S. Roop and Z. Salcic, **DynaGALS Marie Curie Grant**, 2008, EU FP7 program, EUR100,000.
- P. S. Roop, PI, **Game Engineering Using Multiclock Semantics**, FRDF Grant, University of Auckland, $25,000, 2007.
- P. S. Roop, PI, **From High Level Models to Direct Execution Platforms for BHS**, one PhD scholarship, $90,000 Technology in Industry Fellowships funded by Technology New Zealand (collaborative project between Glidepath New Zealand Ltd and University of Auckland).
- P. S. Roop, PI, **Automated ASIP Synthesis from Esterel**, Early Research Career Awards Fund, $70,000, 2003-2005.
- P. S. Roop, PI, **Adaptive Reuse of Embedded Systems**, International Research Collaboration Visits Fund, $4000.00 for research collaboration with A/Professor Arcot Sowmya of University of New South Wales, Australia, 2001.
- P. S. Roop, A. Sowmya, **Controlling Robots to Play Soccer Using Esterel**, University of Auckland Research Fund, $16,000, 2001
- A. Sowmya, S. Ramesh, P. S. Roop, S. Parameswaran, **Component Reuse Framework for Embedded System Design**, UNSW University Research Support Program, AUD20, 000, 2001.

**Supervision**

Completed two Postdocs, seven PhDs and fifteen ME research theses under my main supervision. Two graduated PhD students received Postdoc awards in Europe (INRIA and IBM). One of my earlier Postdocs is now employed as a Senior Lecturer in Lund University, Sweden. Two graduated PhDs are now employed as Senior Lecturer (AUT University) and Lecturer (Auckland University).

Postdoctoral Fellows:

1. Sidharta Andalam, "Heart-on-FPGA FRDF project", Postdoctoral fellow, 2015-2017.

Current Students (PhD):

1. Hugh Wang, "A new design approach for functionally safe medical devices", PhD student, started 2012, (main supervisor).
2. Mahmood Hikmet, "Functionally safe V2V and V2I Networks", PhD student, started 2012, (main supervisor).
3. Jin Woo Ro, "Functionally safe rescue robots", PhD student, 2013 (main supervisor).
4. Neha Sharma, "Optimization of transport control algorithms", 2013 (main supervisor).
5. Hammond Pearce, "Power and timing aware mixed criticality systems", 2015 (main supervisor)
6. Nathan Allen, "Real-time heart models for emulation of pacemakers", 2015 (main supervisor).

Past Students:

Completed PhD students are listed in Table 1 and completed ME students are listed in Table 2.

| Student | Main | Co | Publication | Year | Placement |
|---|---|---|---|---|---|
| Ivan Radojevic | Salcic | Roop | 7 | 2008 | Researcher at NZ Army |
| Avinash Malik | Salcic | Roop | 5 | 2009 | Postdoc at INRIA → Lecturer (Auckland) |
| Roopak Sinha | Roop | Khoussainov | 8 | 2008 | Postdoc (Wellington Drive) → Senior Lecturer (AUT) |
| Li Hsien Yoong | Roop | Salcic | 10 | 2011 | Postdoc (FRDF) → Fusion Transactive |
| Simon Yuan | Roop | Salcic | 4 | 2013 | Navico |
| Gareth Shaw | Roop | Salcic | 4 | 2013 | Navman |
| Sid Andalam | Roop | Biglari-Abhari | 6 | 2013 | Postdoc (UoA) |
| Eugene Yip | Roop | Biglari-Abhari | 3 | 2015 | Postdoc (Bamberg Uni, Germany) |
| Matthew Kuo | Roop | Patel | 5 | 2015 (submitted) | RA in Uniservices |
| Adeel Ali | Roop | Warren | 4 | 2015 (to submit) | CEO (APIMatic) |
| Zeeshan Bhatti | Roop | Khoussainov | 5 | 2015 (to submit) | CTO (APIMatic) |

Table 1: Completed PhD students from 2004-2015

**Scholarships :**

- Australian Development Cooperation Scholarship, 1996. (All India Rank 2nd)
- QIP Scholarship of Govt. of India, 1992.
- Senior Merit Scholarship of Govt. of Orissa.
- M.Tech Research Project at IIT Evaluated as Excellent.

| Student | Main | Co | Publications | Honours |
|---|---|---|---|---|
| Sajeewa Dayaratne | Roop | Salcic | 2 | 1st class |
| Wilfred Wong | Roop | - | 0 | 1st class |
| Li Hsien Yoong | Roop | Salcic | 2 | 1st class |
| Alif Wahid | Roop | Salcic | 1 | 1st class |
| Dong Hui | Salcic | Roop | 3 | 1st class |
| Kent Yap | Roop | Patel | 0 | 1st class |
| Peter Ching | Roop | - | 0 | no |
| Samuel Chen | Roop | Sinha | 0 | no |
| Matthias Schmeling | Roop | Sponemann | 0 | 1st class |
| Rob Connolly | Roop | Salcic | 0 | 1st class |
| Zeeshan Bhatti | Roop | - | 1 | 1st class |
| Hugh Wang | Roop | - | 0 | 1st class |
| Kyle Nicholas | Roop | - | 0 | 1st class |
| Neha Sharma | Roop | - | 0 | 1st class |
| Jin Ro | Roop | - | 1 | 1st class |
| Yu Zhao | Roop | - | 1 | 1st class |
| Bill Collis | Rowe | Roop | 0 | 1st class |

Table 2: Completed ME Students from 2004-2011