Dependable Computing - Understanding Dependability and Fault Tolerance and Implications
(6th February 2018 to 10th February 2018)

Overview:

This course aims at detailed discussion on system to be designed with dependability and fault tolerance. Most of us have experienced a failure of a computer system. Many a times a simple reboot just does the trick. However, the need for reliable systems is everywhere and is becoming very pervasive in everyday life. A good testimony for the need also come from the fact that in many conferences, up to 1/3rd papers are discussing faults, failures, impairment, and similar terms. So why think of fault tolerance as an after though? The system can be designed with dependability as a first class constraint. This course is designed to focus on this topic of importance.

Objectives:

The primary objectives of the course are as follows:

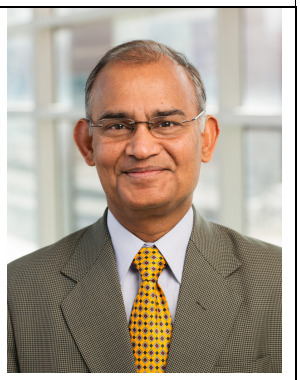
1) Learn the need and methods to achieve fault tolerance in computer systems
2) Redundancy levels and management in hardware, software and information world
3) Reliability and availability evaluation methods, techniques, and tools
4) Design of processor, memory and network systems incorporating fault tolerance

Modules	1) Introduction to faults, errors, failures and reliability analysis methods : Feb 06 2) Hardware redundancy management techniques : Feb 07 3) Software and information redundancy methods : Feb 08 4) Algorithm Based Fault Tolerance : Feb 09 5) Design of fault tolerant processor, memory and networks : Feb 10
You Should Attend if...	• You are executives, engineers and/or researchers in industry and/or R&D labs. • You are a B.E./B.Tech./M.Tech/M.Sc/Ph.D. student or a faculty from an academic institutions and/or technical institution. **(Number of the participants for the course is limited to fifty only)**
Fees	The participation fee (nonrefundable) per person (include high-tea and working lunch) Industry / Research Organization : Rs. 3000 Academic Institution Faculty : Rs. 2000 Students and Host Institute Faculty : Rs. 1000 ** **Notes:** **No TA/DA will be provided to participants.** **No Accommodation will be provided.**

The Expert Faculty

Dr. Arun K. Somani

Associate Dean for Research at College of Engineering (2013-Contd.) and Anson Marston Distinguished Professor (2007-Contd.) at Iowa State University, Ames, IA, USA.



Dr. Arun K. Somani earned his M.S.E.E. and Ph.D. degrees in electrical engineering from the McGill University, Montreal, Canada, in 1983 and 1985, respectively. He also worked as Scientific Officer, Department of Electronics, Govt. of India, New Delhi during (1974-82), a faculty member at the University of Washington, Seattle, WA (1985-97), Chair of the Department of Electrical and Computer Engineering at Iowa State University (2003-2010), Ram Rajindra Malhotra Professor (2010-11), Indian Institute of Technology, Delhi, and the Chair of the HPC steering committee to develop a sustainable model to support high-performance computing (HPC) infrastructure, during 2012-2015.

Professor Somani's research interests are in the areas of dependable and high performance system design and architecture, wavelength-division multiplexing-based optical networking, and image-based navigation techniques in GPS denied environment.

Professor Somani designed and built a scale-able multi-computer architecture termed Proteus, for U.S. Coastal Navy in 1990-92. This design was implemented for the Navy by Applied Physics Laboratory at the University of Washington, Seattle. He was the lead designer of an anti-submarine warfare system for Indian navy, Meshkin, fault-tolerant computer system architecture for the Boeing Company, Proteus multi-computer cluster-based system for US Coastal Navy, and HIMAP design tool for the Boeing Company.

Professor Somani has received several accolades for his technical, research, and leadership contributions. He is a Fellow of IEEE, a Fellow of AAAS, and a Distinguished Engineer of ACM.

Course Coordinator

Dr. D. A. Parikh is an associate Professor in the Department of Computer Engineering at L. D. College of Engineering. His research areas include computer network, wireless networking, and software engineering.

Short Term Course On

Dependable Computing - Understanding Dependability and Fault Tolerance and Implications

06th February - 10th February, 2018

at

L D College Of Engineering
Ahmedabad

Patron

Dr. G. P. Vadodariya
Principal
L D College Of Engineering

Course Coordinator

Dr. D. A. Parikh
Associate Professor
Department Of Computer Engineering
L D College Of Engineering, Ahmedabad
Phone : +91-9426310994
Email : **daparikh@ldce.ac.in**

Course Co-coordinator

Prof. T. J. Raval
Associate Professor
Department Of Computer Engineering
L D College Of Engineering, Ahmedabad
Phone : +91-9825395959
Email **: tushar.raval@ldce.ac.in**

Registration (offline)

Download Registration form and Submit with DD in favor of “Principal, L D College of Engineering, Ahmedabad”

Contact Information

Phone : +91-9825395959
Email : tushar.raval@ldce.ac.in

Registration Form

Short Term Course on

Dependable Computing - Understanding Dependability and Fault Tolerance and Implications

06th February - 10th February, 2018

1. Name: _____

2. Qualification:_____

3. Designation:_____

4. Institute:_____

5. Address: _____

_____

6.Mobile:_____

7.E-mail: _____

8. Fee Details: (Use SBI online link)

Rs._____ Date of online payment:_____

Date: Signature of Applicant

Place: Signature of sponsoring authority & Seal

Important Dates

Last date for Registration :	**06/01/2018**
Short-listed participants list :	**25/01/2018**
Course Date :	**06/02/2018 to 10/02/2018**

Fees

The participation fee (nonrefundable) per person is
Industry / Research Organization : Rs.3000
Academic Institution Faculty : Rs.2000
Students and Host Institute Faculty : Rs.1000

No TA/DA will be provided to participants.
No Accommodation will be provided.

How to Apply?

Interested participants are requested to download Registration form from college website www.ldce.ac.in and submit with online payment through SBI online link https://www.onlinesbi.com/prelogin/institutiontypedisplay.htm

It should reach us on or before 20th January 2018. Participant should send Hard copy and dully filled scanned copy of the registration form to **tushar.raval@ldce.ac.in** with subject line as "GIAN-STC-2018". Apply as soon as possible before the last date of the registration, because only **50** seats are available**. Selection will be based on first come first serve basis.**

Venue

Upanishad Hall
Computer Engineering Department
L D College of Engineering,
Navarangpura,
Ahmedabad-380015.

Contact Details

Prof. T. J. Raval
Mobile : +91-9825395959
Phone : +91-79-26306752, 26300735
(Ext. 1236, 1234)
Email : tushar.raval@ldce.ac.in
Computer Engineering Department
L D College of Engineering
Navaranpura, Ahmedabad-380015